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VS

Docket No. 9792909-4023 PATENT

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re U.S. Patent Application of:
Hajime Nakayama

Serial No.: 09/210,540 Examiner: D. Kang

Filed: December 14, 1998 Group Art Unit: 2811

For: SEMICONDUCTOR DEVICE



**RESPONSE**

Assistant Commissioner for Patents
Washington, DC 20231

Dear Sir:

In response to the Office Action mailed October 19, 2001, please consider the following remarks. Enclosed is a Petition for a one month Extension of Time and a check for the requisite fee, so that the period for response runs to and includes March 19, 2002.

Currently pending are claims 1 and 3-11. The claims relate to an improved semiconductor device having a pair of element formation regions separated by an element isolation region. The device employs a pair of gate electrodes containing impurities of different conductivity types. Connected to the gate electrodes are one set of the ends of a pair of impurity storage regions. The impurity storage regions are arranged in a direction different from the direction of the arrangement of the gate electrodes.

The other set of ends are *electrically* connected to one another, for example, through a conductive layer. (Claim 3) As explained at page 11, lines 11-15, "Note that, while not illustrated, a tungsten silicide or other metal silicide is formed by the self-aligned silicate technique on the polycrystalline silicon layer 1 and *electrically* connects the p-type gate electrode 2 and the n-type gate electrode 3. . ." (Emphasis added.)

In contrast, the impurity storage regions are *physically* connected to each other by a semiconductor layer. For example, the semiconductor layer can be formed of polycrystalline silicon, and the gate electrodes and impurity storage regions can be formed by selectively implanting impurities to the polycrystalline silicon layer. (Claim 9)

The application's discussion of the prior art centers on a "so-called two-layer 'polycide' structure of a metal silicide layer and polycrystalline silicon layer for their gate electrodes . . ." (Page 1, lines 11-14.) The application explains, "Note that the gate electrodes 101 and 102 are *electrically* connected with each other by a metal silicide layer formed on the polycrystalline silicon interconnection layer 106 . . ." (Page 2, lines 14-18, emphasis added.) Accordingly, the application, and in particular prior art Fig. 2, do not teach using a semiconductor layer to provide an *electrical* connection between PMOS and NMOS. Instead, the electrical connection is made by a metal silicide layer.

The examiner rejected all the claims under 35 U.S.C. §103(a) as being unpatentable over Jung in view of admitted prior art ("APA"). Figure 1 of Jung shows a semiconductor device having two element formation regions separated by an element isolation region. The semiconductor device contains a pair of L-shaped gate electrodes 12 and 22 *electrically* connected by metal wiring As appreciated by the examiner, the electrodes are not *physically* connected by a semiconductor layer. (Paper __, page 3.)

The examiner suggests that:

> "APA teaches in Fig. 2 using a semiconductor layer to provide an electrical connection between PMOS and NMOS. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a semiconductor layer as taught by APA to provide electrical connection between gates of NMOS and PMOS in Jung's device. One of ordinary skill in the art would have recognized that the semiconductor layer and metal are an art recognized functional equivalent for providing electrical connection and therefore an obvious expedient."
>
> (paper __, pages 3 and 4)

Applicant respectfully disagrees. As discussed above, Fig. 2 does not suggest using a semiconductor layer to provide an electrical connection between PMOS and NMOS. Instead, the

electrical connection is provided by a metal silicide layer. Therefore, it would not have been obvious to use a semiconductor layer to provide an electrical connection between gates of NMOS and PMOS in Jung's device. While one of ordinary skill in the art might have recognized that a metal silicide layer and the metal are functional equivalents, there is no such equivalency between the semiconductor layer and the metal. Therefore, the proposed combination of Jung and the admitted prior art would not have suggested claims 1 and 9-11, so that the rejection of these claims under 35 U.S.C. §103(a) should be withdrawn.

## CONCLUSION

In light of the foregoing amendments and remarks, it is believed that the application is in condition for allowance, so that a prompt and favorable response is respectfully submitted.

Respectfully submitted,

SONNENSCHEIN NATH & ROSENTHAL

March 18, 2002

By: _____
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I hereby certify that this document and any fee being referred to as attached or enclosed is being deposited with the United States Postal Service as first class mail in an envelope addressed to Assistant Commissioner for Patents, Washington, D.C. 20231, on

March 18, 2002 _____
Date Kathleen Gaines

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